21.4 A Receiver with Start-up Initialization and Programmable Delays for Wireless Clock Distribution

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With the increase of clock frequency for microprocessors, clock distribution has become challenging due to decreasing allowable clock skew and jitter, and the increased impact of dispersion [1, 2]. To address these, a clock based on distribution of a mono-tone sine wave with a frequency 8 times of the actual clock frequency has been investigated [3]. The sine wave can be distributed using electromagnetic waves transmitted from an on-chip antenna [4, 5] as well as using conventional metal interconnects. Using a mono-tone sine wave greatly reduces the impact of dispersion. As will be discussed, the frequency divider with programmable delays in a clock receiver also should allow the clock skew to be compensated within 3.125% or 1/32 of a clock period. Lastly, the wave transmission with an antenna should also free up wires for other uses.

In such systems, however, distributed clock receivers start up with random phases. Additionally, the varying distances and metal structures between the transmitting and receiving antennas make the transmitted signal arrive at different receivers with varying delays and amplitudes. These result static skew. To lower the start-up skew, an initialization approach has been demonstrated in a compact clock system with an external antenna that can synchronize ~4× the area thought possible at ~ 3GHz [6]. In this paper, an 18GHz clock receiver is reported. It is fabricated in an 8M 0.13µm CMOS process to evaluate the feasibility of the clock concept that implements the initialization approach with a clock detector/initialization circuit, and includes a frequency divide-by-8 circuit with 16-programmable quantized delays. The receiver generates a 2.25GHz local clock. The divider enables the skew caused by the varying distances and metal structures between antenna pairs to be compensated within 1/32 of a period of the local clock. As the transmission frequency is increased with the scaling to accommodate higher local clock frequency, the compensation accuracy of this technique should scale.

Figure 21.4.1 shows a block diagram of the system. In the transmitter, a VCO generates a sine wave and an output buffer amplifies the signal. In addition, a control circuit halts the wave transmission for 1.3ns every 30ns [6]. On the receiver side, an LNA with a 3dB bandwidth of 5GHz [7] amplifies the received signal (Fig. 21.4.2), and feeds it to a detector/initialization circuit and a frequency divide-by-8 circuit with programmable delays. The broadband/low-Q amplifier (Q=1.4) reduces the distortion of received signal with the no transmission period. The detector generates a pulse (INI) from the no transmission period. At the rising edge of the INI, the divider loads the programmed delay for skew compensation. Following the falling edge of INI, at the first crossing point of the received clock signal (Fig. 21.4.1), the divider starts with the count down of the programmed delay. This relaxes the pulse (INI) timing accuracy requirement to around a period of the 18GHz transmitted sine wave.

The detector (Fig. 21.4.3) uses envelop rather than edge detection to accommodate the rise and fall times of tuned circuits and antennas (~1 to 2 periods of the 18GHz signal). The envelop detector generates two outputs (OUT1/OUT2). Removing the dc component using a bias circuit creates two crossing points (t_1, t_2) associated with the termination and initiation of clock transmission. A 5-stage buffer is used to amplify the detected signal [8]. The second stage contains clamping PMOS transistors to reduce the effects of input amplitude variations.

The divide-by-8 circuit (Fig. 21.4.4) consists of 3 stages of programmable divide-by-2 circuits. The output of each divide-by-2 circuit can be shifted by 180° using the program bits P_n, n=2,3,4. The first stage consists of two divide-by-2 circuits (Fig. 21.4.4), driven by 180° phase shifted inputs, and generates 90° phase shifted outputs (Q_1/Q_2). By switching the inputs to the second divider stage between Q1 and Q2 using P_1, the 16-step programming is implemented. The circled transistors provide feedback for zero-latency transition from program cycle to normal operation mode and for reducing the input amplitude sensitivity. The divider works from 17 to 18.7GHz. Figure 21.4.4 also shows that when the input amplitude is varied from 0.18 to 0.5V, the measured skew of divider output is ~5 ps, which is tolerable.

Figure 21.4.5 shows the die micrographs of the transmitter and the receiver with 2mm zigzag dipole antennas. The transmitter and receiver areas excluding bond pads and empty areas are 0.91 and 1.14mm^2, respectively. The measurement setup is shown in Fig. 21.4.1. The separation between the antennas is 260µm. To match to the operating frequency range of the receiver, a synthesizer is used to provide the 17 to 18.7GHz clock signal to the transmitter. The control signal for generation of the no-clock transmission is used to trigger an Agilent 86100B oscilloscope. Figure 21.4.6 shows the triggering signal, the receiver output with a programming period, and the transmitter output signal used to drive the antenna. At 18GHz, the transmitter output power is ~4dBm, the antenna pair gain (G_a) [4] is -22dB, and the LNA voltage gain is 19dB.

Figure 21.4.7 also shows the receiver outputs for varying programming bit (P_1-P_4) settings, when the system is working at 18GHz. Figure 21.4.7 also shows that the differences between the expected and measured delays are less than 3.5ps, demonstrating the proper programming operation. The programmed delays can be determined using either an open- or a closed-loop technique to compensate the system skew within ~14ps. The measured jitter including the noise generated by the transmit buffer and receiver is ~5ps$_{p\text{-}p}$. Because the system is initialized every ~30ns, the jitter also includes the uncertainty associated with initialization and programming. Since the jitter is measured in the absence of large digital circuits, it is an optimistic estimate. However, compared to the reported jitters measured in similar situations, the ~5-ps$_{p\text{-}p}$ jitter is competitive.

Using an off-chip PA that increases the transmitted power to 11dBm, the system is demonstrated at 2.5mm separation between a transmitting antenna and a receiver. Currently, the range is limited by the insufficient LNA gain and low transmitted power. Increasing the LNA gain by 20dB will raise the receiver power consumption from 50 to ~80mW at the 0.13µm node. With the transmitter power consumption of 60mW and 16 receivers to distribute the clock signal across an 18×18 = 324mm^2 chip, the total area and power consumption for the global clock distribution will be 19mm^2 and 1.3W, respectively. The power consumption is small compared to that of a clock for high-performance microprocessors.

References:

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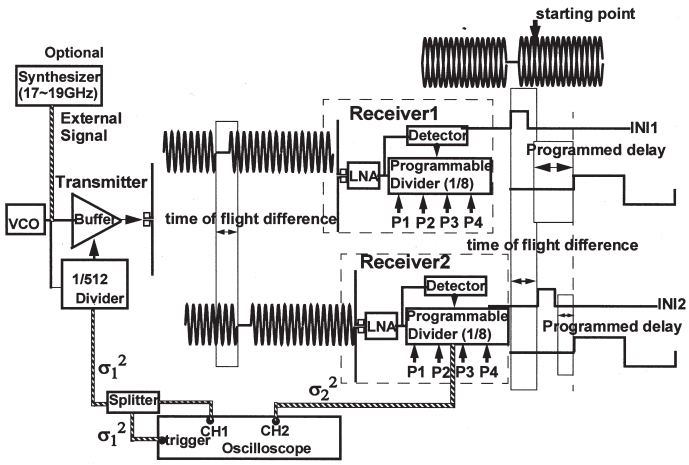

Figure 21.4.1: Synchronization scheme, block diagrams of TX and RX, and measurement setup.

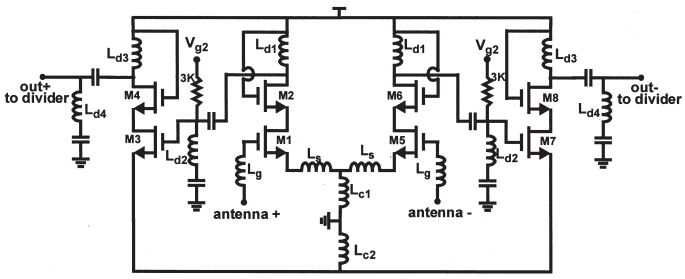

Figure 21.4.2: A schematic of a 2-stage differential low-Q LNA.

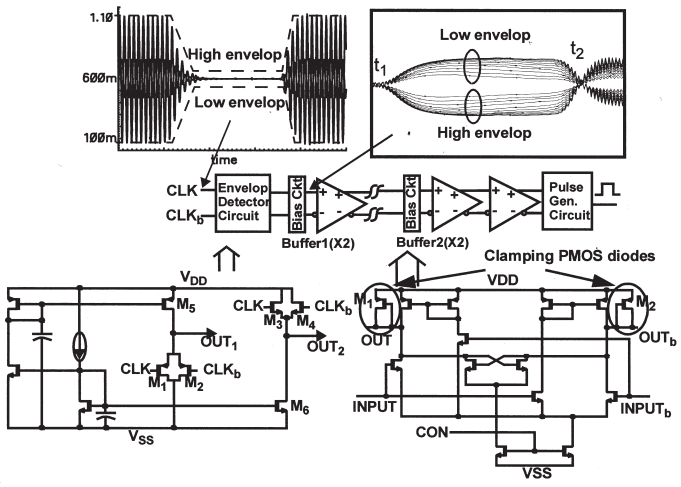

Figure 21.4.3: A schematic of envelop detector/pulse generator.

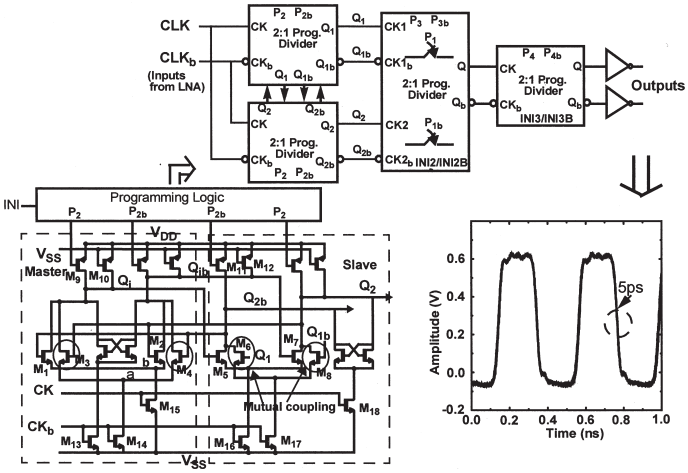

Figure 21.4.4: A schematic of the programmable divider and the output wavwforms of the divider when the divider input amplitude changes from 0.18V to 0.5V.

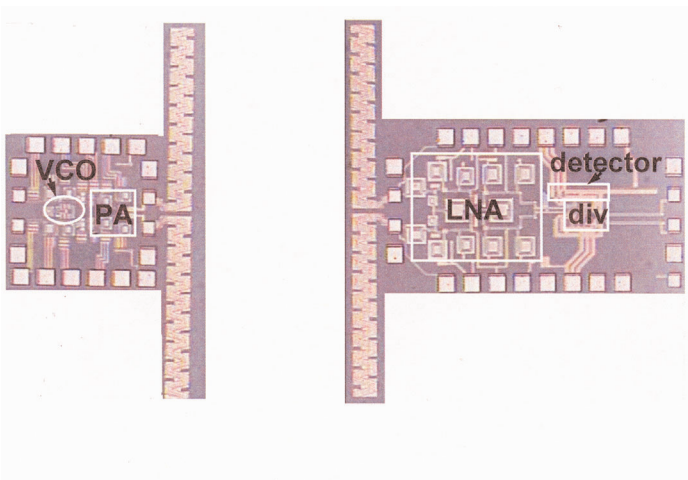

Figure 21.4.5: Die micrographs of a transmitter and a receiver.

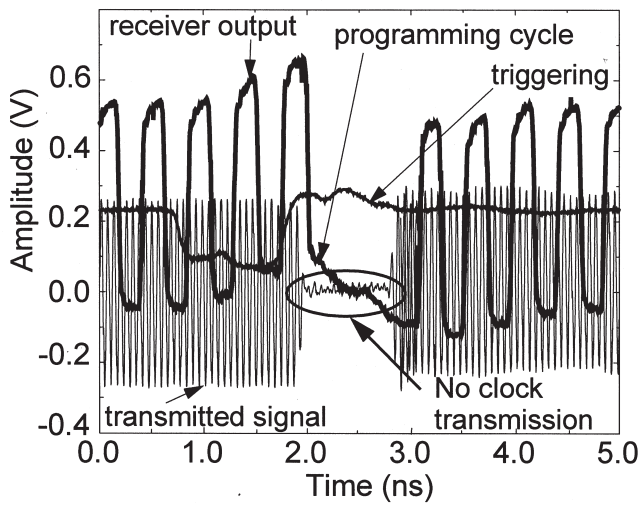

Figure 21.4.6: The transmitted signal, triggering signal and receiver output signal.

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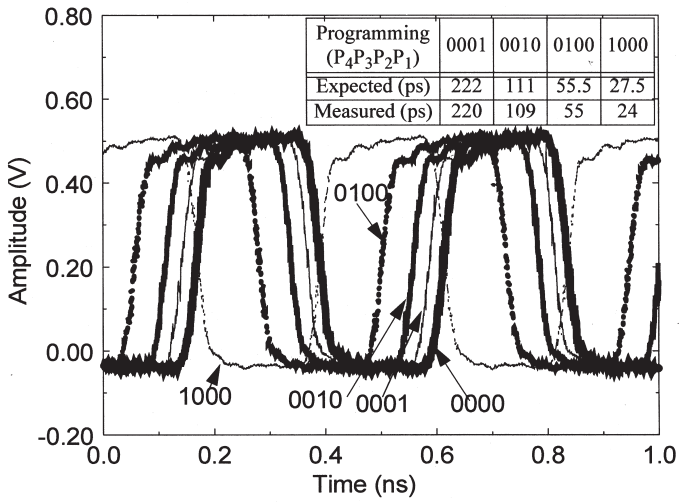

Figure 21.4.7: The receiver output as function of program bit settings.

